

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	102	703/14.ccls. and @pd>"20070201"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/07/20 16:30

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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L7	467	cache near test\$3 and @ad<"20040301"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/07/20 16:38
L8	223	(cache near test\$3) and cache.ti. and @ad<"20040301"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/07/20 16:48
L9	31	(cache near test\$3) and (cache near10 simulat\$4) and @ad<"20040301"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/07/20 16:48


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CL Su, AM Despain - ... of the 1995 international symposium on Low power design, 1995 - portal.acm.org

 ... of Embedded Processors," IEEE **Design & Test** of Computers, Vol. 11, No. 4, pp. 24-31, Dec. 1994. [11] CL Su and Alvin M. Despain, "Cache Designs for Energy ...

 Cited by 200 - [Related Articles](#) - [Web Search](#)
Adaptive mode control: A static-power-efficient cache design - all 18 versions »

H Zhou, MC Toburen, E Rotenberg, TM Conte - ACM Transactions on Embedded Computing Systems (TECS), 2003 - portal.acm.org

 ... 3, August 2003. Page 11. Adaptive Mode Control: A Static-Power-Efficient **Cache**
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 Cited by 86 - [Related Articles](#) - [Web Search](#)
[book] Principles of CMOS VLSI design: a systems perspective - all 4 versions »

NHE Weste, K Eshraghian - 1985 - Addison-Wesley Longman Publishing Co., Inc. Boston, MA, USA

 ... on **Design**, automation and **test** in Europe, p.591-598, March 27-30, 2000, Paris, France. Tony D. Givargis, Jörg Henkel, Frank Vahid, Interface and **cache** power ...

 Cited by 1155 - [Related Articles](#) - [Web Search](#) - [Library Search](#)
[book] Computer organization & design: the hardware/software interface - all 16 versions »

DA Patterson, JL Hennessy - 1993 - Morgan Kaufmann Publishers Inc. San Francisco, CA, USA

 ... Tony Givargis, Improved indexing for **cache** miss reduction in ... of the 40th conference on **Design** automation, June ... Instruction-level DFT for **testing** processor and ...

 Cited by 810 - [Related Articles](#) - [Web Search](#) - [Library Search](#)
SimpleScalar: an infrastructure for computer system modeling - all 19 versions »

T Austin, E Larson, D Ernst - Computer, 2002 - ieeexplore.ieee.org

 ... fast mechanism for **design** and **test** provides shorter ... Power-perfor- mance **design** tradeoff

 studies can be per ... issue width, instruction window size, **cache** size, and ...

 Cited by 387 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)
[book] Testing semiconductor memories: theory and practice

AJ van de Goor - 1991 - John Wiley & Sons, Inc. New York, NY, USA

 Cited by 441 - [Related Articles](#) - [Web Search](#) - [Library Search](#)
The directory-based cache coherence protocol for the DASH multiprocessor - all 3 versions »



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- ☐ 1. **Verifying a multiprocessor cache controller using random test generation**
 Wood, D.A.; Gibson, G.A.; Katz, R.H.;
Design & Test of Computers, IEEE
 Volume 7, Issue 4, Aug. 1990 Page(s):13 - 25
 Digital Object Identifier 10.1109/54.57906
[AbstractPlus](#) | [Full Text: PDF\(920 KB\)](#) IEEE JNL
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- ☐ 2. **Performance analysis and its impact on design**
 Bose, P.; Conte, T.M.;
Computer
 Volume 31, Issue 5, May 1998 Page(s):41 - 49
 Digital Object Identifier 10.1109/2.675632
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(148 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ 3. **An integrated functional performance simulator**
 Bechem, C.; Combs, J.; Utamaphethai, N.; Black, B.; Blanton, R.D.S.; Shen, J.P.;
Micro, IEEE
 Volume 19, Issue 3, May-June 1999 Page(s):26 - 35
 Digital Object Identifier 10.1109/40.768499
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(1292 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ 4. **Using a soft core in a SoC design: experiences with picoJava**
 Dey, S.; Panigrahi, D.; Li Chen; Taylor, C.N.; Sekar, K.; Sanchez, P.;
Design & Test of Computers, IEEE
 Volume 17, Issue 3, July-Sept. 2000 Page(s):60 - 71
 Digital Object Identifier 10.1109/54.867896
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(120 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ 5. **Variability in architectural simulations of multi-threaded workloads**
 Alameldeen, A.R.; Wood, D.A.;
High-Performance Computer Architecture, 2003. HPCA-9 2003. Proceedings. The Ninth International Conference on
 2003 Page(s):7 - 18
 Digital Object Identifier 10.1109/HPCA.2003.1183520